FIG. 1

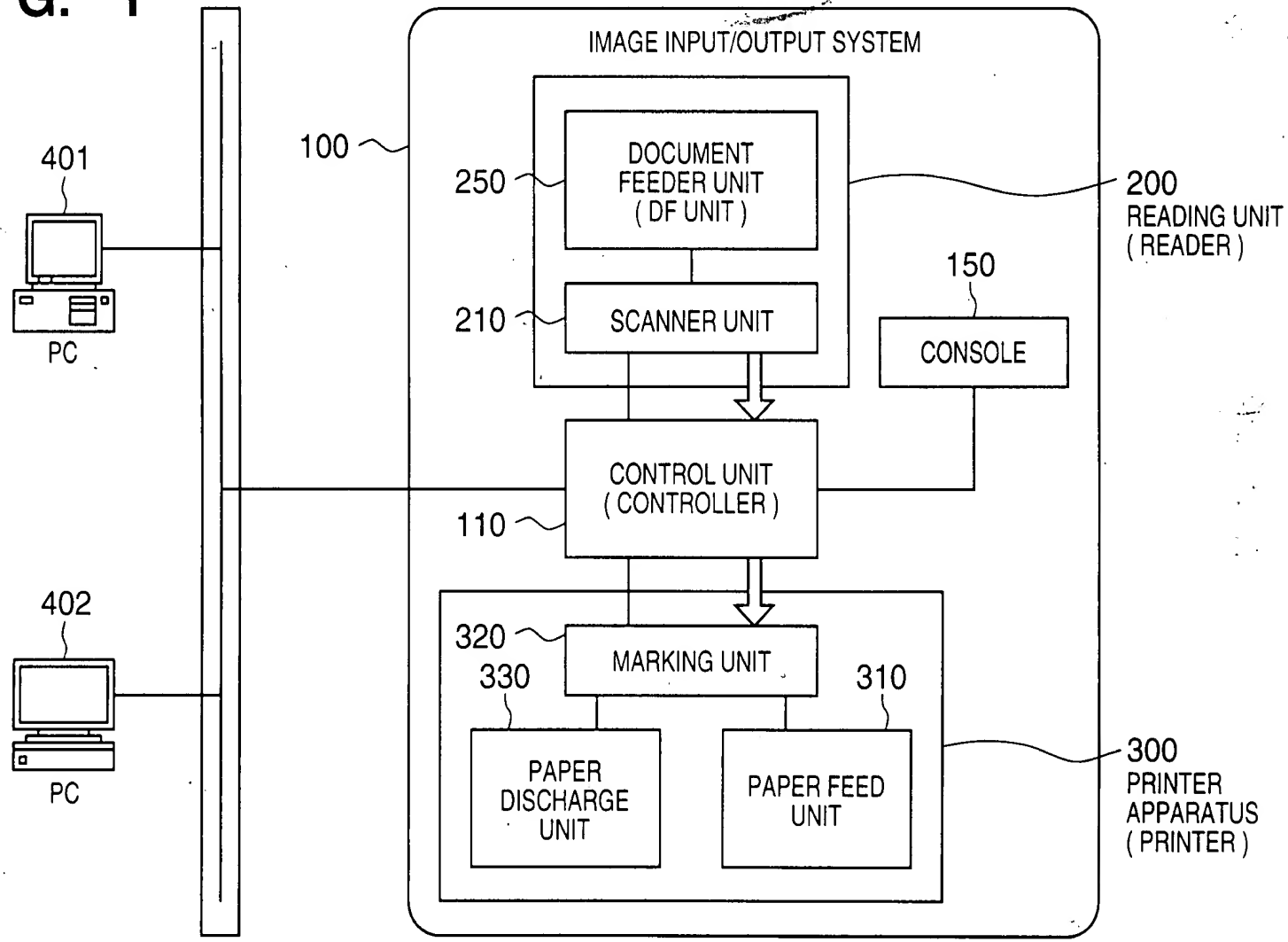


FIG. 2

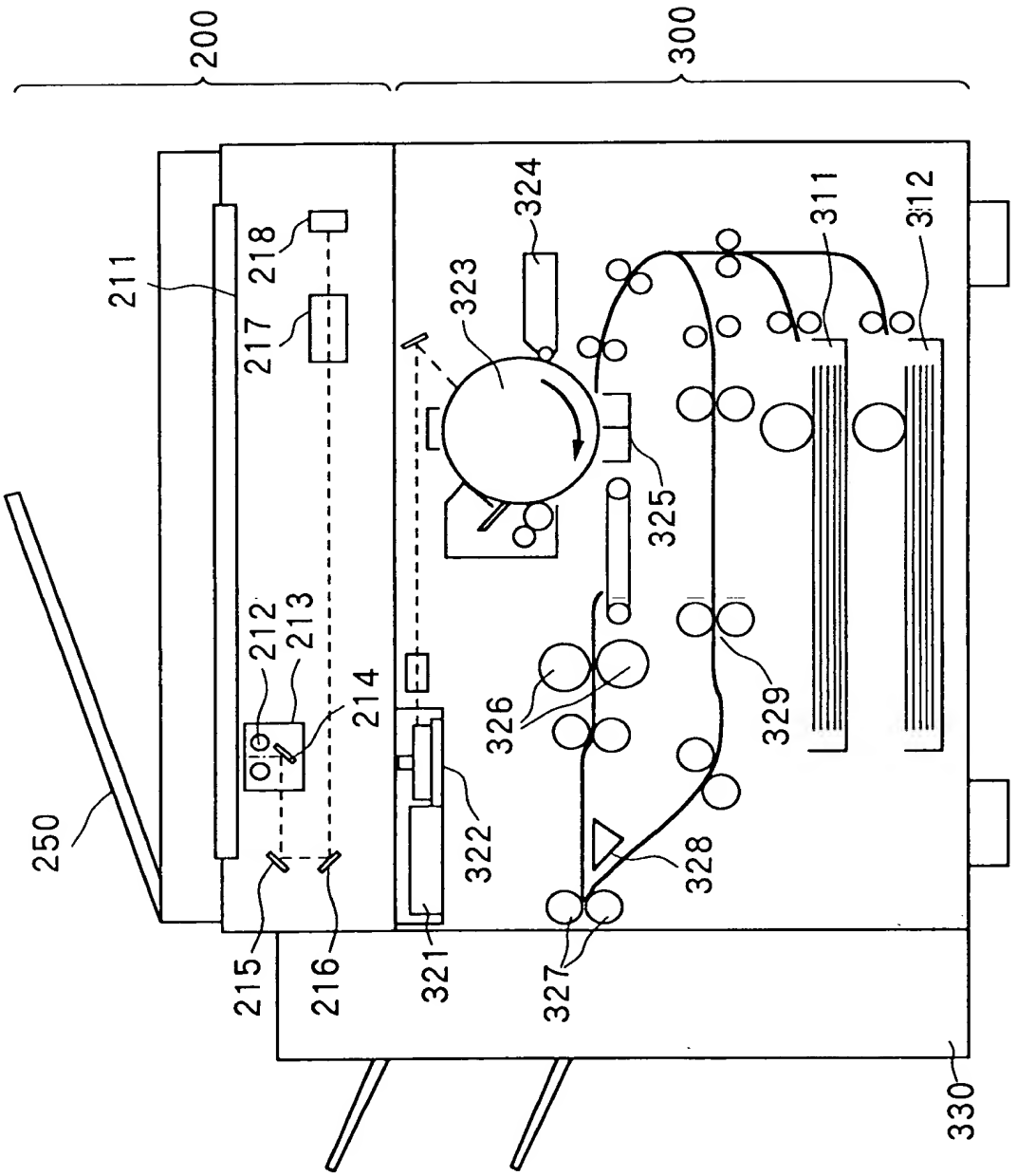

200
300
211
218
217
212
213
214
215
216
250
321
322
323
324
325
326
327
328
329
311
312
330

FIG. 3

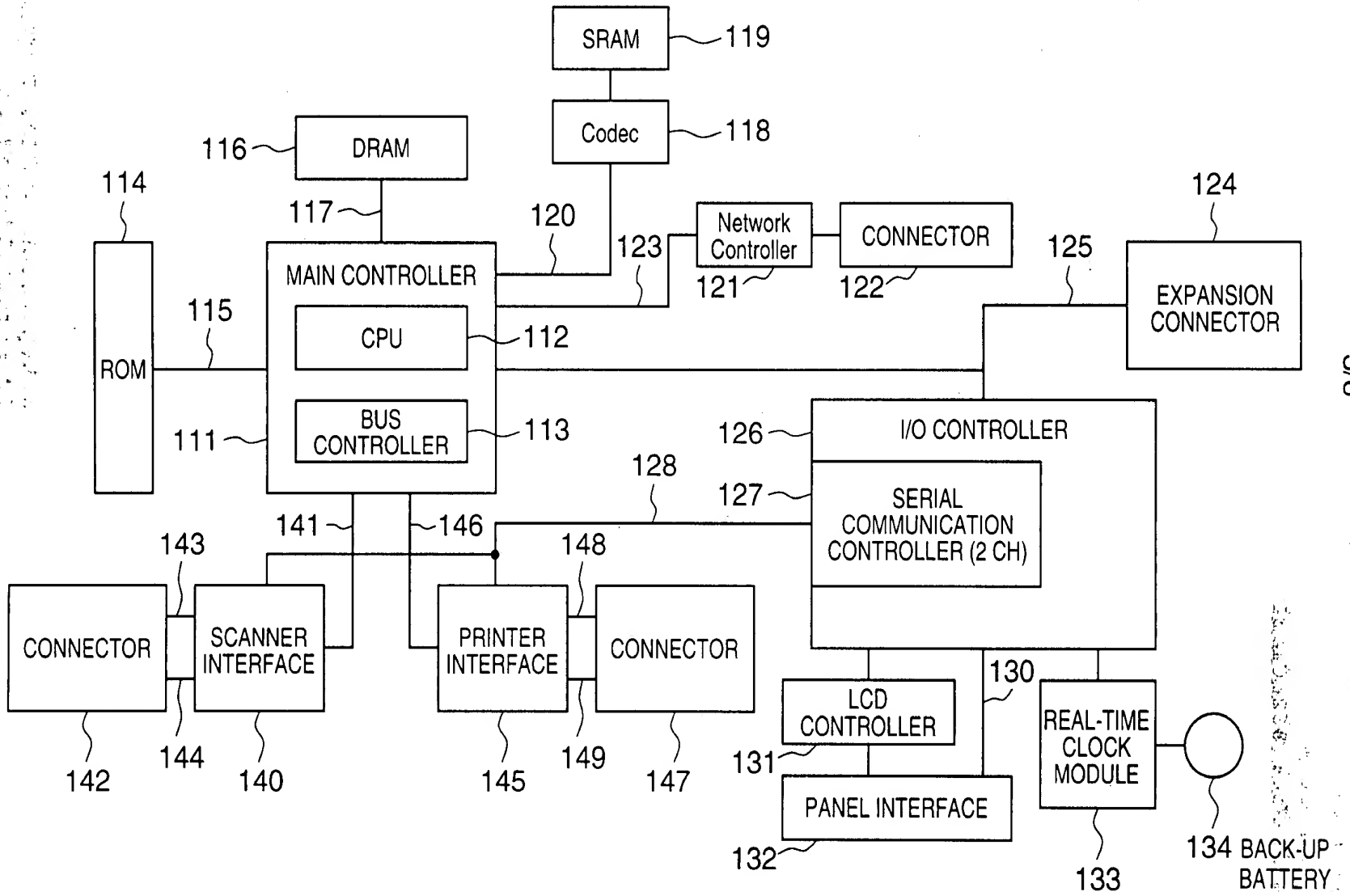

SRAM
119
Codec
118
116
DRAM
114
117
120
123
Network Controller
121
CONNECTOR
122
124
125
EXPANSION CONNECTOR
MAIN CONTROLLER
CPU
112
115
ROM
BUS CONTROLLER
113
111
126
I/O CONTROLLER
128
127
SERIAL COMMUNICATION CONTROLLER (2 CH)
141
146
143
148
CONNECTOR
SCANNER INTERFACE
PRINTER INTERFACE
CONNECTOR
130
LCD CONTROLLER
131
REAL-TIME CLOCK MODULE
PANEL INTERFACE
132
133
134
BACK-UP BATTERY
142
144
140
145
149
147

FIG. 4

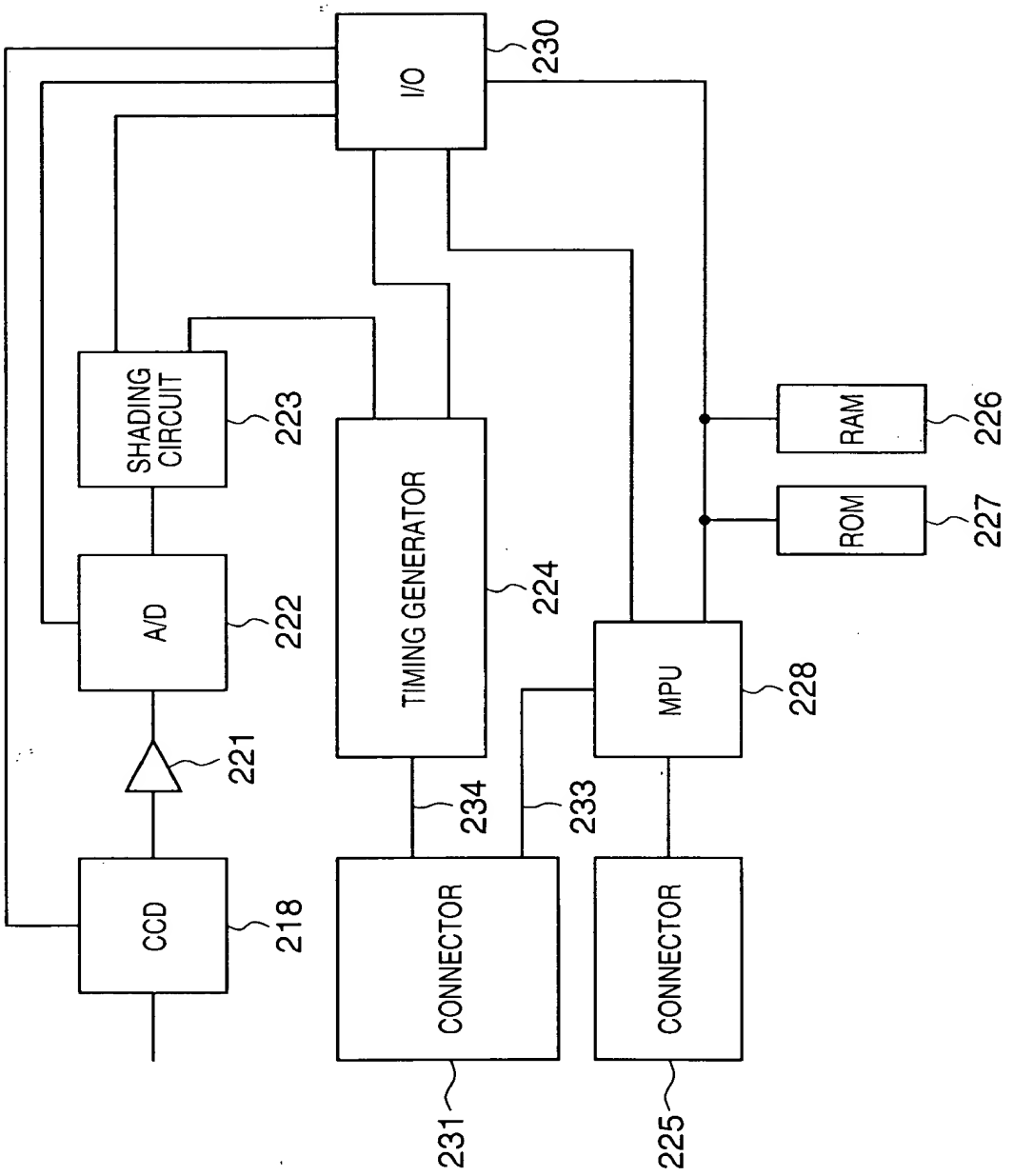

I/O
230
SHADING CIRCUIT
223
A/D
222
221
CCD
218
TIMING GENERATOR
224
MPU
228
RAM
226
ROM
227
234
233
CONNECTOR
231
CONNECTOR
225

FIG. 5

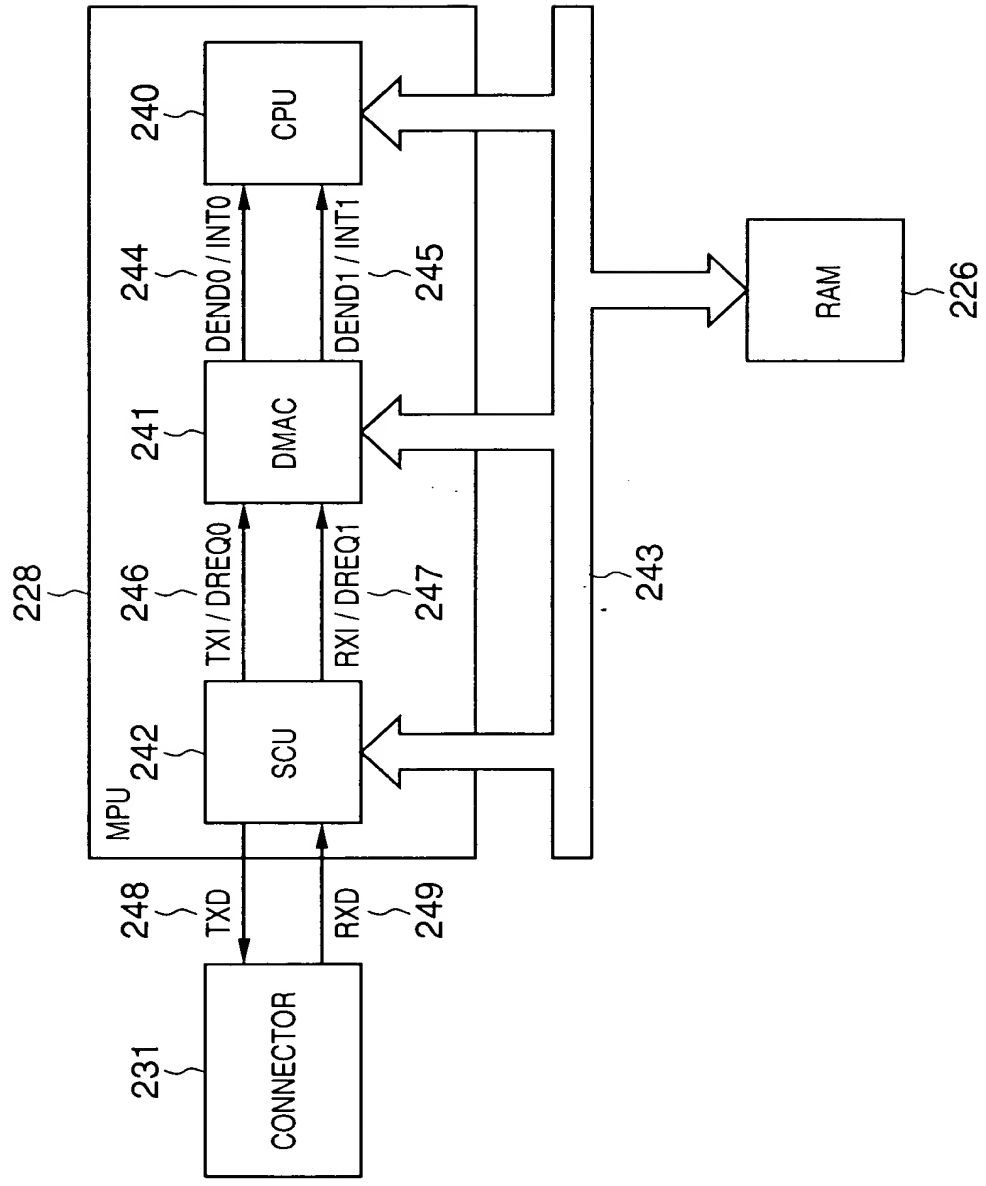

228
MPU
240
CPU
241
DMAC
242
SCU
244
DEND0 / INT0
245
DEND1 / INT1
246
TXI / DREQ0
247
RXI / DREQ1
243
248
TXD
249
RXD
231
CONNECTOR
RAM
226

FIG. 6A

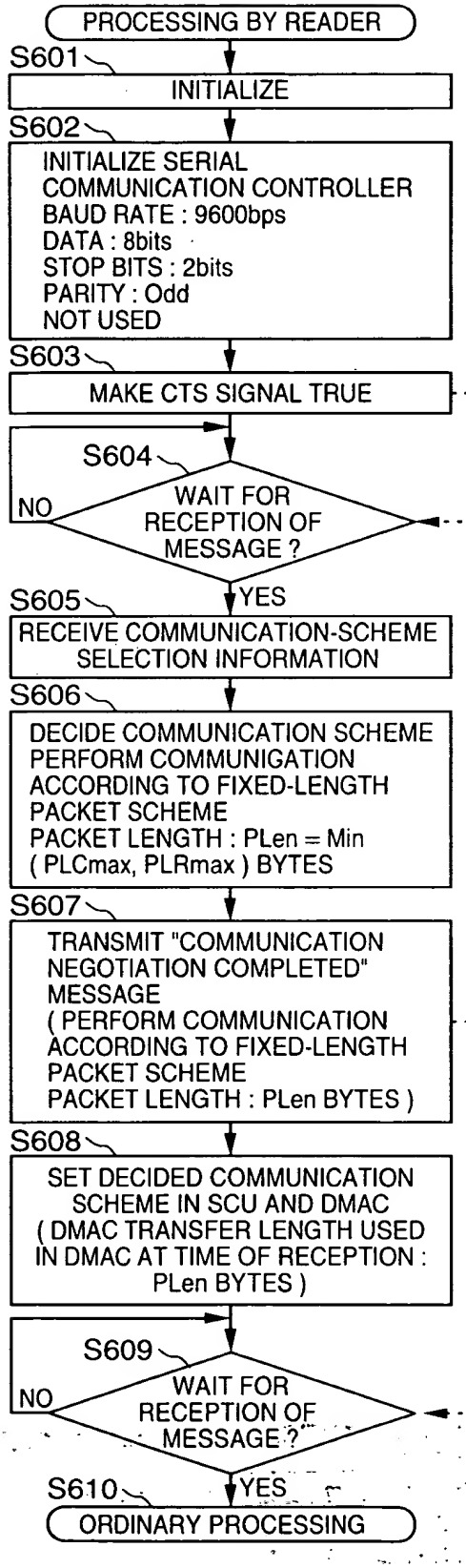


FIG. 6B

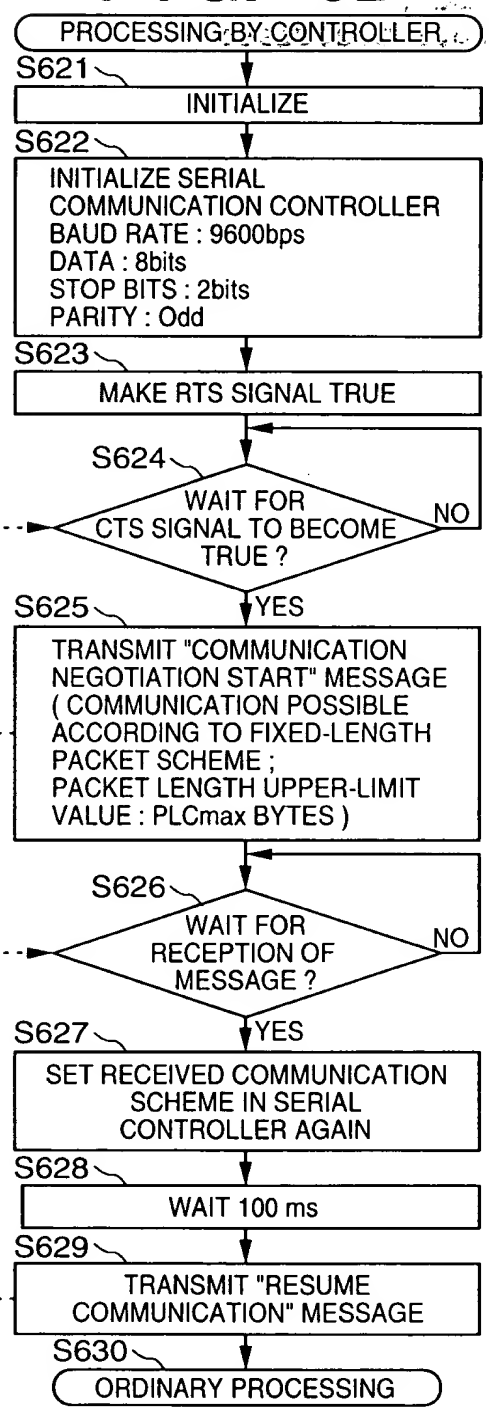


FIG. 7A

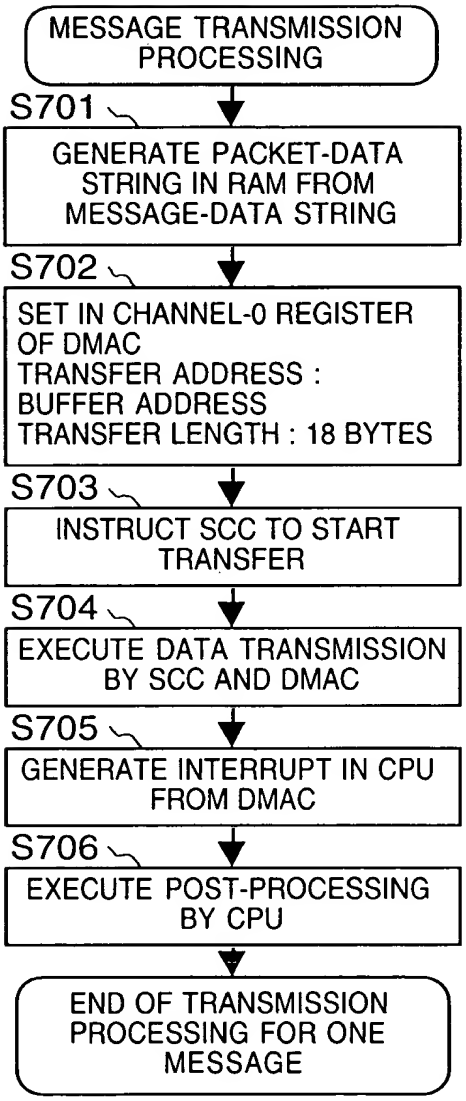

MESSAGE TRANSMISSION PROCESSING
S701
GENERATE PACKET-DATA STRING IN RAM FROM MESSAGE-DATA STRING
S702
SET IN CHANNEL-0 REGISTER OF DMAC
TRANSFER ADDRESS : BUFFER ADDRESS
TRANSFER LENGTH : 18 BYTES
S703
INSTRUCT SCC TO START TRANSFER
S704
EXECUTE DATA TRANSMISSION BY SCC AND DMAC
S705
GENERATE INTERRUPT IN CPU FROM DMAC
S706
EXECUTE POST-PROCESSING BY CPU
END OF TRANSMISSION PROCESSING FOR ONE MESSAGE

FIG. 7B

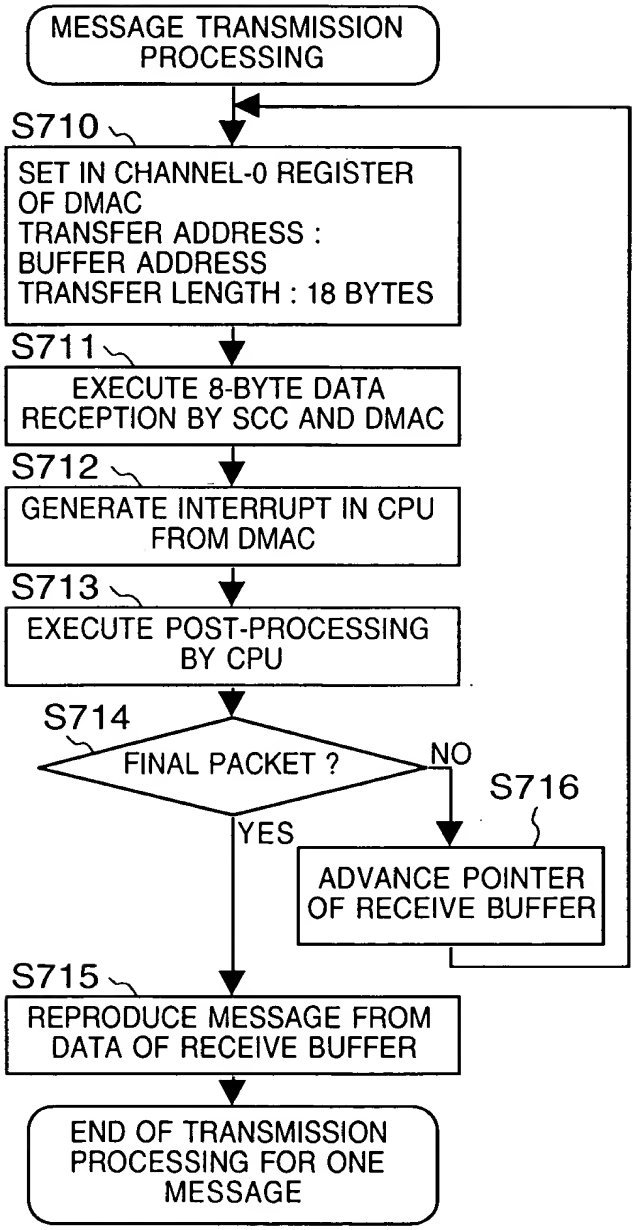
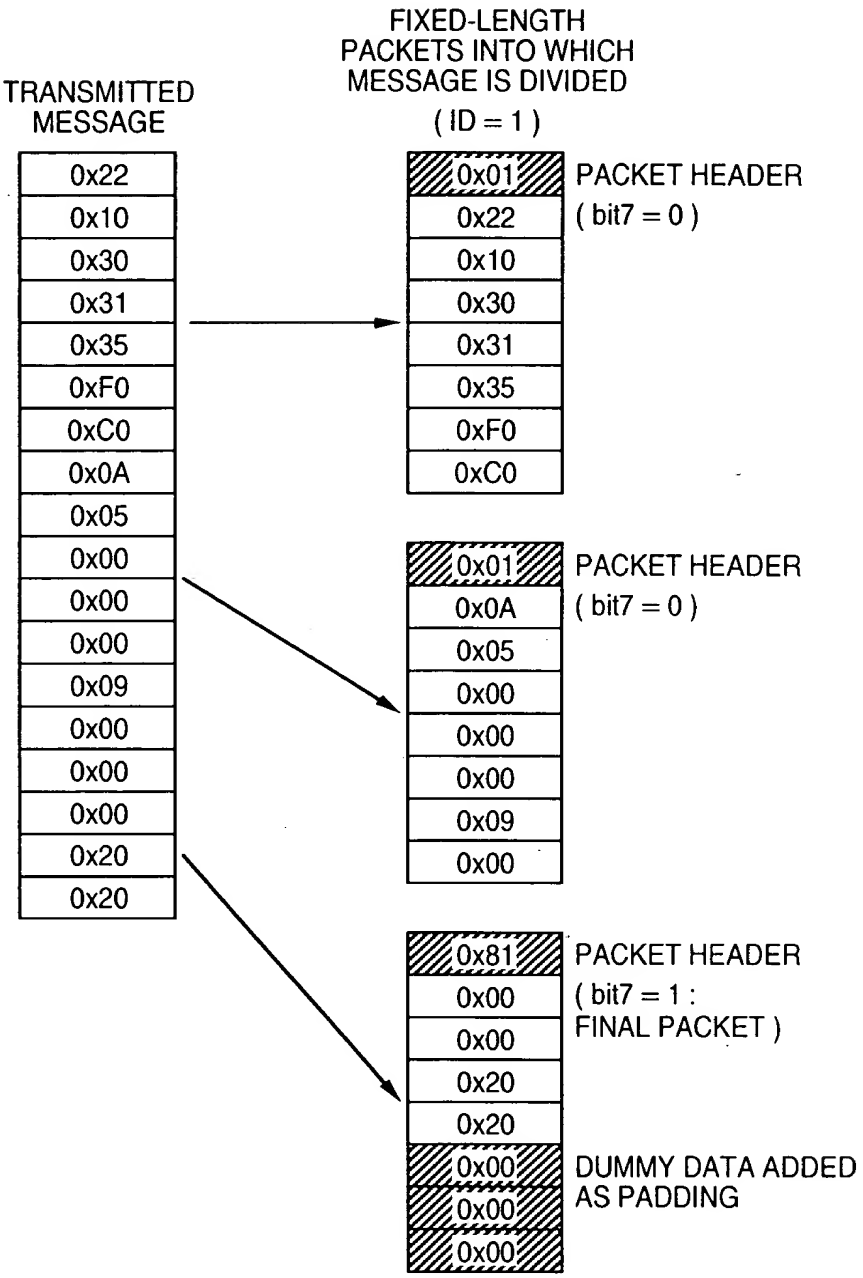

MESSAGE TRANSMISSION PROCESSING
S710
SET IN CHANNEL-0 REGISTER OF DMAC
TRANSFER ADDRESS : BUFFER ADDRESS
TRANSFER LENGTH : 18 BYTES
S711
EXECUTE 8-BYTE DATA RECEPTION BY SCC AND DMAC
S712
GENERATE INTERRUPT IN CPU FROM DMAC
S713
EXECUTE POST-PROCESSING BY CPU
S714
FINAL PACKET ?
NO
YES
S716
ADVANCE POINTER OF RECEIVE BUFFER
S715
REPRODUCE MESSAGE FROM DATA OF RECEIVE BUFFER
END OF TRANSMISSION PROCESSING FOR ONE MESSAGE

FIG. 8


TRANSMITTED MESSAGE
0x22
0x10
0x30
0x31
0x35
0xF0
0xC0
0x0A
0x05
0x00
0x00
0x00
0x09
0x00
0x00
0x00
0x20
0x20
FIXED-LENGTH PACKETS INTO WHICH MESSAGE IS DIVIDED
(ID = 1)
0x01
PACKET HEADER
(bit7 = 0)
0x22
0x10
0x30
0x31
0x35
0xF0
0xC0
0x01
PACKET HEADER
(bit7 = 0)
0x0A
0x05
0x00
0x00
0x00
0x09
0x00
0x81
PACKET HEADER
(bit7 = 1 : FINAL PACKET)
0x00
0x00
0x20
0x20
0x00
0x00
0x00
DUMMY DATA ADDED AS PADDING